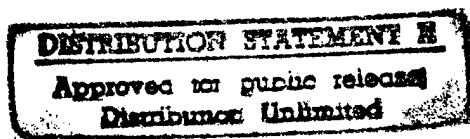# Quarterly Technical Report

Defects and Impurities in 4H- and 6H-SiC Homoepitaxial Layers: Identification, Origin, Effect on Properties of Ohmic Contacts and Insulating Layers and Reduction

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13. ABSTRACT *(Maximum 200 words)*

Chemical vapor deposition systems are being fabricated to deposit 4H- and 6H-SiC thin films at moderate and very high temperatures. Single crystalline AlN films with smooth surfaces were grown using gas-source MBE and characterized with RHEED, XRD, TEM and SIMS. The C-V characteristics of Al/AlN/SiC heterostructures depended strongly on temperature from 200 to 573 K and exhibited hysteresis effects consistent with the presence of slow interface traps. The AlN/SiC interface had a density of trapped negative charge of 3×10^{11} cm^{-2} at 27 °C; it decreased with increasing temperature. A three-step process involving surface preparation, initial insulator formation, and oxide deposition was developed for investigation of oxide growth on 6H- and 4H-SiC. Films of SiO_2 have been deposited at ~10 Å/min for characterization. Measured impact ionization coefficient data indicate that the reverse breakdown voltage of 6H- and 4H-SiC devices should increase with temperature. This data shows that Baliga's figure of merit increases by ~1.5 and ~1.8 for 6H- and 4H-SiC, respectively, indicating superior specific on resistance for SiC field effect transistors relative to that projected earlier. Electron inversion layer mobilities of 110 cm^2/Vs (the highest reported to date) and 160 cm^2/Vs (the first reported value) have been measured in 6H- and 4H-SiC lateral MOSFETs. The devices were fabricated using a non-selfaligned process. A low temperature deposited oxide (LTO) subjected to different oxidizing and inert anneals was used as the gate dielectric.

14. SUBJECT TERMS
silicon carbide, aluminum nitride, SiC, AlN, chemical vapor deposition, heterostructure, interface traps, oxidation, SiO_2, impact ionization coefficient, reverse breakdown voltage, figure of merit, on resistance, transistors, mobility, inversion layer, MOSFET

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I. Introduction

The two most important materials-related problems affecting the performance of all SiC devices and their associated components (e.g., contacts) are the defects and the undesired impurities which become incorporated in the homoepitaxial SiC layers in which all devices are currently fabricated. Bhatnagar [1] has shown that the reverse blocking leakage current in high voltage Schottky diodes is three orders of magnitude higher than theoretically predicted as a result of defects in the epi-layer. The formation of micropipes, stepped screw dislocations, interacting dislocation loops, polyganized networks of dislocations and growth twins as well as stacking faults during the sublimation growth of SiC boules are likely the root cause of some of the defects in the epitaxial layer. However, with the exception of the micropipes, the types and concentrations of line, planar and other three-dimensional defects and their effect on the performance of devices and individual device components in the important epi-layer have not been similarly determined. As such, it is not known which of the latter defects actually are translated from the wafer into the epi-layer during its deposition and, therefore, should be vigorously controlled during boule growth and which defects are generated during deposition.

The relatively uncontrolled occurrence of the n-type donor of N and deep level compensating impurities such as Ti in the epilayer have been identified via secondary ion mass spectrometry, photoluminescence and cathodoluminescence investigations. However, the origins of essentially all of these impurities are unknown. For high-temperature, -power and -frequency devices, it is highly desirable to control or eliminate these impurities such as to attain undoped films with uncompensated carrier concentrations of 10^{14} cm^{-3}—two orders of magnitude lower than what is, at present, normally achieved in standard commercial depositions.

The formation of low resistivity and thermally stable ohmic contacts to 4H- and 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have an advantage over Si, the contact resistivities must be below 1×10^{-5} W-cm^2, as noted by Alok, *et al.* [2]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on low melting point Al or Al alloys to dope the SiC surface below the contacts. These materials are not suitable for devices intended for high-temperature operation. While the fabrication of ohmic contacts to SiC has also normally depended on the attainment of a very heavily-doped near-surface region, the introduction during deposition of high levels of dopants in the near surface device region of the epi-layer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice.

Based on all of these issues and recent experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

To fabricate most microelectronic devices, the growth or deposition of stable insulators is needed to provide both passivating layers and gate dielectrics. Silicon carbide is almost invariably thermally oxidized, albeit at a slower rate, in the same manner and temperature range that is employed for Si. Most of the previous studies regarding the oxidation of SiC have been concerned with polycrystalline materials. It has been shown by Harris and Call [3] and Suzuki, *et al.* [4] that the (0001) face of 6H-SiC oxidizes according to the same linear-parabolic equation reported for Si by Deal and Grove [5]. The model states that the initial stage of oxidation is reaction rate limited and linear, but becomes parabolic as the diffusion of the oxidant through the oxide becomes the rate limiting factor. Research at NCSU by Palmour, *et al.* [6] has demonstrated that the oxidation process on SiC in wet and dry oxygen and wet argon obeys the linear-parabolic law. Both wet processes had a slower rate than dry oxidation at 1050°C and below. The dry oxides exhibited a very flat surface; in contrast, SEM and TEM revealed that wet oxidation preferentially oxidizes dislocation bands, causing raised lines on the oxide and corresponding grooves in the SiC. It was proposed that the much higher solubility of H_2O in SiO_2 as compared to that of O_2 allows wet oxidation to be preferential.

All of the oxidation studies on all polytypes of semiconductor quality SiC have been conducted on n-type material with the exception of the investigation by Palmour *et al.* [6]. The objective of this study was the determination of the redistribution of the common electrical dopants of N, P, Al and B during thermal oxidation of SiC films at 1200°C in dry O_2. Experimental segregation coefficients and interfacial concentration ratios were determined. Secondary ion mass spectrometry revealed that B and Al depleted from the SiC into the growing oxide while N and P were found to pile up in the SiC as a result of the loss of the SiC to the oxide formation. Aluminum is now used almost universally as the p-type dopant in SiC. The electrical properties of oxides thermally grown on n-type SiC normally have reasonably favorable characteristics of high breakdown voltage and low leakage currents. However, the reverse is true for thermally grown oxides on p-type SiC, as shown by Baliga and his students at NCSU. It is believed that at least two of the causes of the poor performance on a p-type material are the existence of the Al in the oxide and at the oxide/SiC interface and the dangling oxygen bonds which this species creates in the oxide as a result of a difference in oxidation state (+3) compared to that of Si (+4) and the existence of C at the SiC/insulator interface. Methods of effectively cleaning SiC surfaces prior to oxidation to deposit and grow oxides on p-type material under UHV conditions and determine the effect of Al redistribution and C concentrations at the interface on the properties of the oxide must be determined. In addition,

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the effect of existing line and planar defects in the SiC epi-layer on the properties of the thermally grown and deposited oxide must be ascertained.

The research conducted in this reporting period and described in the following sections has been concerned with (1) the determination and employment of an effective, completely dry, *ex situ* hydrocarbon and oxide removal process for the 6H-SiC(0001) surface, (2) design and construction of a new CVD SiC system for the deposition and doping of 6H- and 4H-SiC and AlN films, (3) deposition, annealing and electrical characterization of Ni, NiAl, Au, Pt and Cr-B contacts to p-type SiC(0001), and (4) fabrication, for the first time, of high voltage Schottky barrier diodes on 4H- and 6H-SiC(0001) and determination of the associated barrier heights, series resistance and critical electric field strength for breakdown as a function of T. The following individual sections detail the procedures, results, discussions of these results, conclusions and plans for future research. Each subsection is self-contained with its own figures, tables and references.

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II. Growth Via Hot Wall Chemical Vapor Deposition and Characterization of 6H- and 4H-SiC and AlN Thin Films

A. Introduction

A silicon carbide system is being built in order to grow silicon carbide thin films of high quality. A design has been developed. Most parts have been received and have been assembled, and construction is currently under way on the electrical and gas lines.

B. Experimental Procedure

The system design is comprised of a six-way cross, serving as a loadlock, from which two separate chambers are attached. Off of this loadlock, to one side, is a growth chamber. To another side, perpendicular to the axis of the loadlock and growth chamber, is another chamber where RHEED analysis will be performed. The sample will be transferred to and from the various chambers on a SiC-coated graphite susceptor platform on which the sample will be placed. The transfer mechanism consists of a platform which is moved from chamber to chamber by means of a manipulator rod, which is screwed to the side of the susceptor.

The growth chamber consists of a rotating module, to which the susceptor is attached. Growth will occur on the sample in an upside-down position, with gases flowing upward, while the susceptor is being rotated. The susceptor is attached to the rotating rod assembly by a groove into which the susceptor slides when transfer of the sample takes place. Once the sample is transferred to the rotating rod, the rod is brought down to the quartz portion of the reaction chamber. Here, the sample is heated via RF coil, and gases are introduced from the bottom of the reactor. A design which incorporates a graphite cylinder for hot wall CVD growth is in progress. Discussions with various sources on the optimum design for hot wall growth are in progress at this time. Growth temperature will be monitored by means of a standing pyrometer mounted outside the quartz chamber and aimed at the sample. Growth processes, such as gas flow rate and pressure, will be monitored by electronic components. Gas flow will be controlled by mass flow controllers, and pressure by capacitance manometers.

The RHEED (reflection high-energy electron diffraction) chamber, attached on another side of the loadlock chamber, will be attached to monitor film crystallinity, crystal structure and the formation of new surfaces. Since attempts will be made to grow high-quality crystalline SiC films, a RHEED chamber which is attached to a nominal high vacuum to prevent direct exposure to atmosphere after growth will be useful to characterize the film.

The SiC growth process will consist of introducing SiH_4 and C_2H_4 as the reactive components carried by a H_2 carrier. Nominal flow values will be on the order of 1 to 10 sccm for each. Carrier flows of H_2 will be on the order of 3 liters per minute. Other gases which will

be included on the system will be NH_3 and an N_2/H_2 mixture, for doping, and Ar. TEA will also be used for doping, which will be kept at constant temperature by a heater bath.

C. Results

Accomplishments to date include the following:

- A design has been developed where sample transfer, growth, and RHEED analysis have been determined,
- A support frame to provide physical support to the system has been designed and built,
- Three six-way crosses have been installed with the adjoining gate valves on the frame, and available flanges and window ports have been attached,
- A quartz chamber-to-cross assembly has been machined which will provide a sealed interface between two parts of the growth chamber,
- Quartz cylinders have been cut to design dimensions,
- Flange parts, pressure gauge attachments, pump connection parts, and a rotating rod assembly have been machined,
- An RF generator to be used to provide RF heating to the susceptor has been refurbished and returned,
- Assembly of a switch panel to control the nupro valves and to enable computer control has been completed,
- A RHEED chamber manipulator is being fitted with a holder which will accommodate the susceptor upon transfer,
- Electrical wiring of the switch panel to control the nupro valves has been assembled,
- Various gas lines on a panel to be mounted on one side of the system have been arranged,
- Installation of electrical and water utilities for the system, as well as safety changes in the laboratory have been requested.

D. Discussion

The proposed design was developed with many sources of input. A number of constraints determined the design configuration and materials used in the system.

One of the main concerns was the high operating temperature of the growth chamber. Since temperatures around 1600-1700°C were going to be used to grow SiC thin films, it was determined that quartz would be the best material for the growth portion of the chamber. Once this was determined, a design had to be developed to cool the chamber. A double-walled quartz vessel, water cooled around the perimeter, was determined to be the optimum mode of cooling. A hot wall CVD system was determined to be the best method for achieving a high growth rate. Discussions are underway at this time to design the most appropriate graphite inner chamber inside the quartz cylinders for this purpose.

Another concern was the transfer mechanism of the susceptor and the placement of samples on the susceptor surface. It was decided that small silicon carbide screws would be the most flexible to accommodate various sized samples. For the transfer mechanism, a simple tongue-in-groove assembly, moved between chambers by means of a transfer arm which would screw into the side of the susceptor, was deemed simplest and most practical.

E. Conclusions/Future Research Plans and Goals

A system design for the deposition of SiC thin films has been developed. Most components have been designed or received. Other needed parts are currently being machined. A graphite inner chamber is being devised to accommodate hot wall CVD growth. Further assembly of the system is expected when electrical and water sources to the laboratory enable start up of many parts of the system.

III. Growth of SiC and AlN by Gas-Source Molecular Beam Epitaxy

A. Introduction

Thin films of SiC and AlN, two important materials in current semiconductor research, have recently been grown by gas-source molecular beam epitaxy (GSMBE) under this program [1-4]. A partial list of the results from these studies include the following: i) Single-crystalline films of 3C-SiC(111) and 6H-SiC(0001) were grown on 6H-SiC (0001) substrates. Polytype and growth rate were controlled by substrate orientation, substrate temperature and gas phase chemistry [5]. ii) Single-crystalline AlN films were deposited on vicinal and on-axis 6H-SiC(0001) wafers using aluminum evaporated from an effusion cell and nitrogen derived from either an electron cyclotron resonance plasma source or NH_3. In general, AlN films <50 Å had higher defect density on vicinal 6H-SiC than on nominally on-axis 6H-SiC [2]. iii) Single-crystal heterostructures and solid solutions of AlN and SiC were also achieved. Superior AlN/SiC multilayers were realized when very thin AlN layers were deposited on on-axis 6H substrates. Single-phase solid solutions of AlN_xSiC_{1-x} were deposited for 0.2<x<0.8. A transition from the zincblende to the wurtzite structure was observed at x=0.25 [6,7].

At the moment, wurtzite AlN thin films are grown in the GSMBE system. The AlN layers are, for instance, an interesting alternative to silicon dioxide in high temperature SiC devices. The structure, chemical purity, and electrical properties of the AlN films are investigated.

B. Experimental Procedure

The growth is conducted in a GSMBE system with an ultimate base pressures of 10^{-10} Torr. Prior to growth SiC substrates are cleaned using procedures developed in the group [2]. The SiC films are grown using SiH_4 and C_2H_4 where the gas-flows are accurately controlled by regulating the pressure over a flow-cell. The AlN growth is made by evaporating Al from an effusion cell and simultaneously introducing NH_3 through a mass flow controller. In addition to the gases mentioned above, it is also possible to introduce H_2, N_2 and Ar during growth. The system is equipped with two *in situ* analysis tools. The gases in the chamber are monitored with a 100 AMU residual gas analyzer (RGA). Differential pumping of the RGA makes it possible to record the gas content in the chamber at pressures above 1×10^{-3} Torr. The surface structures are analyzed with reflection high energy electron diffraction (RHEED).

In addition to these *in situ* techniques several *ex situ* analysis techniques are available, for instance, transmission electron microscopy (TEM), x-ray diffraction (XRD), scanning electron microscopy (SEM) and atomic force microscopy (AFM) for structural investigations, Auger electron spectroscopy (AES) and secondary ion mass spectroscopy (SIMS) for chemical analysis, and capacitance-voltage (C-V), current-voltage (I-V) and Van der Pauw Hall measurements for electrical characterization.

C. Results and Discussion

Wurtzite AlN thin films have been grown on vicinal and on-axis 6H-SiC and 4H-SiC substrates. RHEED, XRD and TEM shows that (0001) oriented, single crystalline films with smooth surfaces can be grown on both the vicinal and on-axis SiC surfaces. Roughness measurements using AFM show rms values of 10-15 Å for films grown on on-axis substrates. TEM cross-sections show that films on both vicinal and on-axis substrates are highly (0001) oriented with a high defect density. Efforts are made to reduce the density of defects.

The impurity levels of oxygen and hydrogen in AlN are normally high. The AlN films grown in the GSMBE system have a minimum oxygen and hydrogen content of about 10^{19} cm^{-3}. In order to lower the impurity levels, Al and NH$_3$ with higher purities are presently used. The films will soon be analyzed using SIMS.

Comparison between films grown on Si-face, C-face and non-polar 4H-SiC are made. RHEED images of the films surfaces show that AlN grown on C-face substrates have smooth surfaces. Electrical measurements are made on Al/AlN/SiC MIS-structures.

D. Future Research Plans and Goals

The growth of high-quality AlN layers as a high temperature dielectric on SiC will continue. The effect of H$_2$ and NH$_3$ on the AlN/SiC interface will be studied. Investigations regarding the mechanisms controlling the surface chemical effects of H$_2$ on SiC growth rate and polytype change (3C - 6H or 4H). The growth of SiC on 2H-AlN will be investigated and the achievements of 2H-SiC will be a primary goal in these experiments. These investigations will be used as input for experiments growing 6H-SiC/3C-SiC, 4H-SiC/3C-SiC and AlN/SiC heterostructures. In addition, detailed studies on the growth of AlN$_x$SiC$_{1-x}$ solid solutions will be conducted as a function of AlN concentration.

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IV. Electrical Characterization of Metal/AlN/6H-SiC(0001) Heterostructures

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Abstract – Metal/AlN/n–type 6H–SiC (0001) (MIS) heterostructures have been prepared by epitaxially growing wurtzite AlN layers on both vicinal and on-axis 6H–SiC (0001) substrates using gas-source molecular beam epitaxy. The capacitance-voltage characteristics obtained for these MIS heterostructures are found to depend strongly on temperature in the range from 200 to 573 K, and to exhibit hysteresis effects consistent with the presence of slow interface traps. The amount of hysteresis is found to increase with decreasing temperature. This can be explained in terms of the shift of the Fermi level closer to the semiconductor conduction band with decreasing temperature, causing the emission rate of the trapped charge to be less dependent on temperature. Cross-sectional high-resolution transmission electron microscopy results show that the interface formed on the vicinal 6H–SiC (0001) substrate contains a higher density of defects than that on the on-axis substrate. However, these two interfaces are found to have a similar density of trapped negative charge of 3×10^{11} cm^{-2} at room temperature, which decreases with increasing temperature. These results indicate that the interface between AlN and Si-terminated 6H–SiC (0001) is of a high quality suitable for device application.

I. Introduction

Recently, there has been increasing interest in the electrical properties of silicon carbide (SiC) metal-oxide-semiconductor (MOS) structures because of their applications in high-power and high-temperature devices[1]. The fabrication of these structures is made possible, in part, by the fact that SiC is unusual among wide band gap semiconductors in that it can be thermally oxidized to form silicon oxide (SiO_2) layers with relatively low oxide charge and interface state densities[2]. However, several authors[3]-[5] have reported electrical instabilities in the SiO_2/SiC system. Furthermore, the transconductances of SiC MOS field-effect transistors (MOSFETs) are presently limited by the carrier surface mobility which is degraded by surface roughness and charged interface states[1]. The problems associated with thermally grown oxides, however, may be alleviated by the use of deposited dielectrics[6]. Because of its wide band gap (6.2 eV at 300 K) and low dielectric constant ($\varepsilon_0 = 8.5$)[7], aluminum nitride (AlN) represents an attractive alternative to oxides as a dielectric for SiC-based devices. In addition, AlN normally forms in the hexagonal wurtzite structure and is rather closely lattice-matched to SiC allowing the growth of high-quality epitaxial layers[8].

It has been theoretically shown that for the nonpolar (110) interface between cubic AlN and cubic SiC, the energetically favorable bonding configuration is Si–N and Al–C which corresponds to cation-anion bonding across the interface[9]. It has also been shown that for this bonding configuration, no interface localized states occur in the main band gap, and that dangling

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bonds existing at the SiC (110) surface are almost completely healed at the interface[9]. On the other hand, for nonisovalent systems such as AlN/SiC, abrupt polar interfaces would be characterized by the occurrence of either oversaturated or undersaturated bonds. It is well known[10] from semiconductor interface studies of similar nonisovalent systems (e.g., Ge/GaAs), that this situation would place the system in an unstable state. This has led to the suggestion that atomic intermixing occurs at the interface in such a way as to compensate III-IV and IV-V bonds, thereby avoiding the occurrence of strong electric fields in the system[11]. In fact, Ourmazd et al.[12] showed that atomic intermixing even exists for isovalent systems such as Al_xGa_{1-x} As/GaAs and depends strongly on the growth temperature. From results of high-resolution transmission electron microscopy (HRTEM) studies, Ponce et al.[13] concluded that the most favorable atomic arrangements at the abrupt polar interface between AlN and (0001) Si-terminated 6H–SiC are the intermixed configurations of Si–N and Al–C bonds, which produce no significant changes in the Si–C or Al–N back-bond lengths. Recently, we have shown[14] that the interface formed on n–type 6H–SiC (0001) has a density of trapped negative charge of 1×10^{11} cm^{-2} at room temperature. In this paper, we show that the capacitance-voltage (C-V) characteristics of metal/AlN/n–type 6H–SiC (0001) (MIS) heterostructures depend strongly on temperature and exhibit hysteresis effects consistent with the presence of slow interface traps. We also show that the amount of hysteresis is dependent upon temperature. It has been shown[15] that the presence of particular Si-terminated steps on the vicinal 6H–SiC (0001) surface causes the introduction of defects in the AlN layer that originate at the interface. However, we find that the interfaces formed on both vicinal and on-axis 6H–SiC (0001) substrates have a similar density of trapped negative charge at room temperature, which decreases with increasing temperature.

II. Experimental Procedure

The AlN layers (100 nm thick) were grown on (0001) Si-terminated 6H–SiC substrates at 1373 K using gas-source molecular beam epitaxy (GSMBE)[16]. Sources were Al (99.999 % pure), evaporated from standard effusion cell, and 3.0 sccm ammonia (99.999 % pure). Nitrogen-doped (2×10^{18} cm^{-3}) 6H–SiC wafers containing 0.8-μm-thick epitaxial layers [N-doped to $(2-4) \times 10^{16}$ cm^{-3}] deposited via chemical vapor deposition and thermally oxidized to a depth of 75 nm were used as substrates in this work. The substrates were chemically cleaned in a 10% hydrofluoric acid solution to remove the oxide immediately before they were inserted into the growth chamber. To remove any residual hydrocarbons and oxide prior to deposition, the substrates were further cleaned using a 1-min silane exposure at 1273 K followed by a 10-min anneal at 1523 K in ultrahigh vacuum (1×10^{-9} Torr) until a 1 x 1 reconstruction pattern became visible in the reflection high-energy electron diffraction (RHEED) pattern of the 6H–SiC (0001) surface[17]. In order to investigate the effect of the interfacial defect structure on the C-V characteristics, the AlN layers were grown simultaneously on vicinal (3-4° off (0001) toward [$11\overline{2}0$]) and on-axis substrates at a rate of 100 nm/h. The AlN/SiC interface was examined by cross-sectional HRTEM using 200 KV Topcon 002 B electron microscope. Depth profiles of impurities in the AlN layers were determined by secondary ion mass spectrometry, with a C_s^+ primary ion beam.

The doping profile of uncompensated donors in the epitaxial layers was uniform and their concentration was 2×10^{16} cm^{-3}, as determined from the C-V measurements reported below. The MIS heterostructures were prepared by deposition of circular Al contacts with an area of 5.4×10^{-3} cm^2 on the AlN through a metal mask. Blanket deposition of Al was made on the backside of the wafers to form a large area ohmic contact. The C-V measurements were performed at frequencies between 1 kHz and 1 MHz and at temperatures ranging from 200 to 573 K. The measurements were carried out in the dark with a voltage sweep rate of 100 mV/s. Measurements were also performed as follows: the device was illuminated with light from a halogen lamp while biased in deep depletion, making possible the modulation of the interface trap population. When a stable capacitance value was reached, the bias voltage was swept in the dark into accumulation and back to deep depletion at a sweep rate of 100 mV/s.

III. Results and Discussion

Figure 1 shows cross-sectional HRTEM images of the AlN layer on the on-axis and vicinal 6H–SiC (0001) substrates. The AlN layer grows in a two-dimensional growth mode with a hexagonal wurtzite structure and has an abrupt interface with the 6H–SiC (0001) substrate [Fig. 1 (a)].
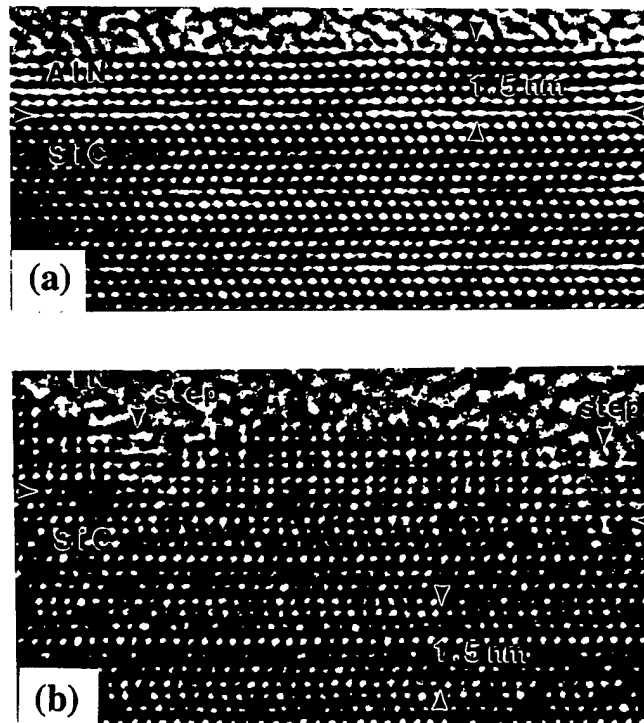

Fig. 1   High-resolution TEM images of the AlN/6H–SiC (0001) interface formed on (a) an on-axis substrate and (b) a vicinal substrate. The arrows shown in (b) indicate the step positions.

However, the misalignment of coalescing AlN island-like areas at steps on the vicinal 6H-SiC surface due to the difference in stacking sequences of the AlN and the SiC results in the introduction of inversion domain boundaries (IDBs) in the AlN layer[15]. The presence of IDBs and the abrupt nature of the interface are revealed in Fig. 1 (b). For the layers used here with a thickness exceeding the equilibrium critical thickness for hexagonal AlN (~ 4.6 nm), threading dislocations that arise from the strain associated with these planar defects and with lattice mismatch are also observed[17].

A typical high-frequency (1 MHz) C-V curve obtained at room temperature for MIS heterostructures formed on a vicinal, n–type 6H–SiC (0001) substrate is shown in Fig. 2. Also shown in Fig. 2 is a theoretical curve calculated[18] for a 100 nm AlN layer on an n–type (2 x 10^{16} cm-3) 6H–SiC (0001) substrate. No frequency dispersion of the capacitance is observed in the frequency range studied here. The C-V curve exhibits no appreciable hysteresis and shows deep depletion for negative gate voltages with no inversion capacitance characteristics observed due to the extremely low minority-carrier generation rate[19]. Figure 3 shows the behavior of the C-V curve when the device is illuminated with light from a halogen lamp while biased in deep depletion. It can be seen that hysteresis now appears in the deep-depletion portion of the curve consistent with the presence of slow interface traps that are not in equilibrium with the Fermi level in our experiment. Illumination results in a reduction of the charge occupancy of these interface traps and as a consequence, for a given bias voltage there is less negative charge in the interface traps on the positively going than on the negatively going voltage sweep. This results in the device capacitance being smaller on the negatively going than on the positively going voltage sweep.
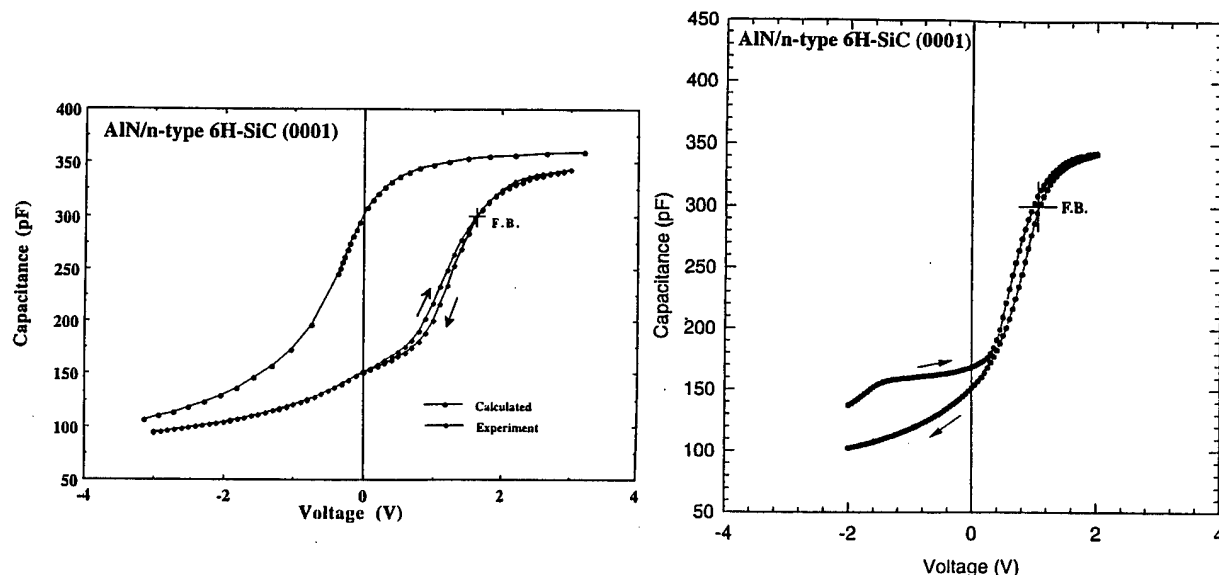
Fig. 2   High-frequency (1 MHz) C-V curve measured at room temperature in the dark with a voltage sweep rate of 100 mV/s and a theoretical curve calculated for a 100 nm AlN layer on an n–type (2 x 10^{16} cm^{-3}) 6H–SiC (0001) substrate.

Fig. 3   Effect of illuminating the MIS device with light from a halogen lamp while biased in deep depletion on the C-V behavior.

Similar hysteresis effects were also observed in silicon MIS structures at low temperatures ($\leq$ 160 K), where the generation of minority carriers is very small and the time constant for the charge emission from interface traps is very long[20].

From Fig. 2, using 4.2 eV for the work function of Al and 3.7 eV for the electron affinity of 6H–SiC (0001)[21], the flatband voltage, V_{FB}, of +1.2 V (determined from the sweep from accumulation to deep depletion) represents a shift of +0.85 V from ideal, for a negative interface charge density of 3 x 10^{11} cm^{-2} at room temperature. Note that interface trap stretchout is not observed in the experimental C-V curve when compared to the ideal curve in Fig. 2. This charge must then reside largely in such slow interface traps.

Figure 4 illustrates the effect of temperature on the C-V characteristics. It can be seen that increasing the temperature has the effect of shifting the curves to less positive gate voltages (or the capacitance to higher values). This shift indicates that less negative charge is trapped at the interface for a given bias voltage as a consequence of the movement of the Fermi level to lower energies with increasing temperature[22]. This behavior is consistent with the presence of acceptor-type traps. At 473 K V_{FB} is almost dominated by the work function difference between Al and 6H–SiC (0001). Note also that as the temperature is lowered below 300 K, the portions of the curves that correspond to depletion exhibit a pronounced hysteresis. It is observed that the amount of hysteresis increases with decreasing temperature, yet one would have thought that the emission rate of the trapped charge would decrease drastically with decreasing temperature and hence, that no substantial hysteresis effects would be manifested in the C-V characteristics. The movement of the Fermi level closer to the bottom of the semiconductor conduction band (note that the interface traps are now filled to a higher level) must then have the effect of causing the emission rate to be less dependent on temperature[22]. The emission rate must also be less than the rate of change of the gate charge in our experiment as evidenced by the hysteresis effects.
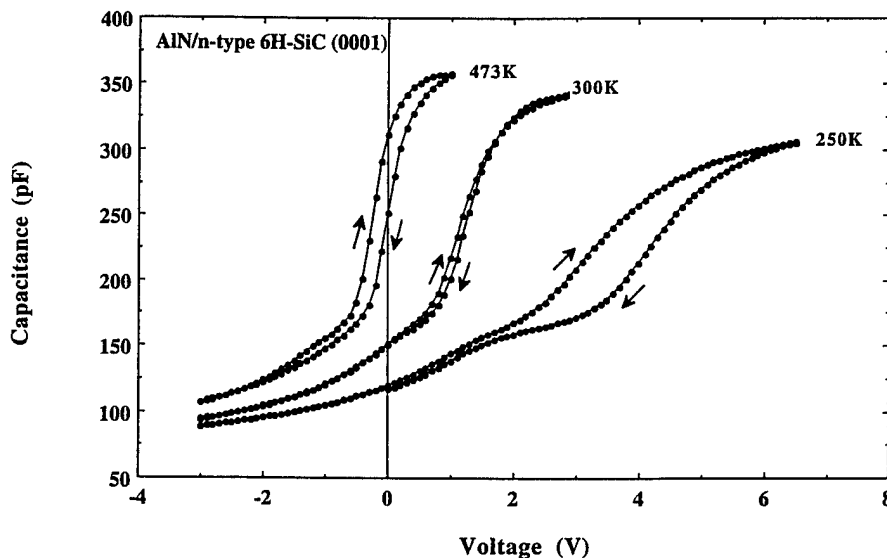

Fig. 4   A set of C-V curves measured at different temperatures in the dark with 'a voltage sweep rate of 100 mV/s.

Furthermore, the reduction of the slopes in the C-V characteristics from the ideal ones with decreasing temperature suggests that charge emission takes place from a continuum of interface traps[22].

It should be emphasized here that regardless of whether the MIS heterostructures are formed on vicinal or on-axis 6H–SiC (0001) substrates, almost identical C-V characteristics are obtained (Figs. 2 and 4). These results are in marked contrast to those reported for thermally grown and deposited oxides on n–type 6H–SiC (0001)[6], [19], which show increased hysteresis, and a shift in the C-V curves to more positive gate voltages as the temperature is increased from 300 to 573 K. This shift indicates that in this case, more negative charge is trapped at the interface due presumably to a larger number of slow interface traps being thermally excited[19].
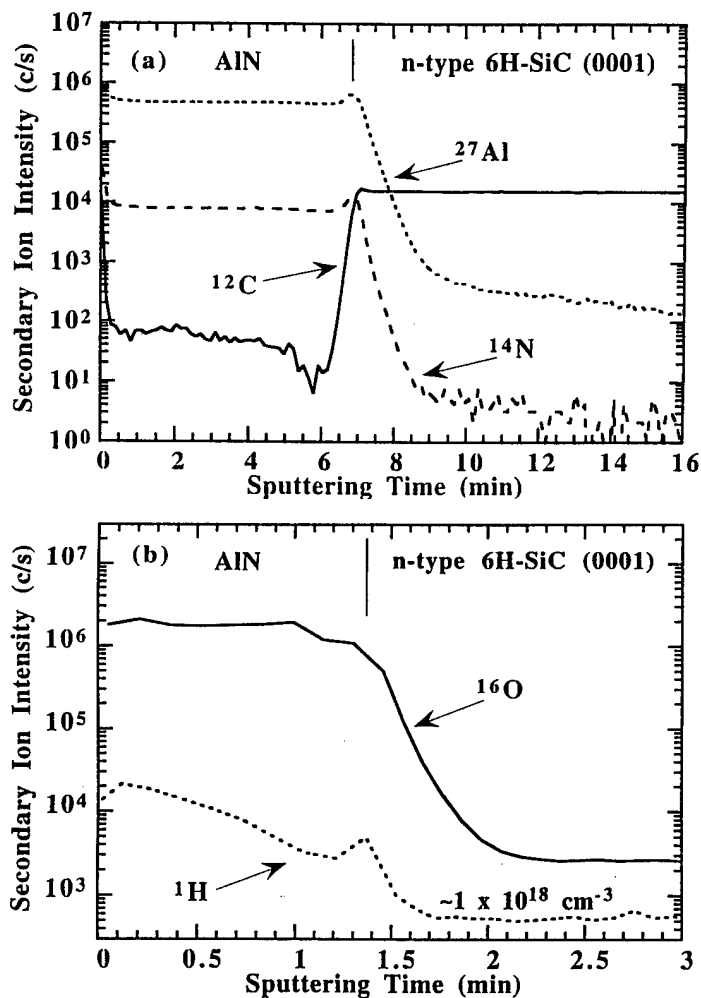

Fig. 5   SIMS depth profiles of (a) carbon, (b) oxygen and hydrogen in an AlN/6H–SiC (0001) heterostructure. The carbon concentration in the AlN layer is estimated to be about 10^{16} atoms/cm^3. The oxygen and the hydrogen concentration is estimated to be about 10^{19} atoms/cm^3 using the background signals in the 6H–SiC substrate. The apparent Al signal in the substrate is due to the interference of the NC signal and does not indicate the diffusion of Al into the 6H–SiC substrate.

Although high-resolution TEM images show that the interface formed on the vicinal 6H–SiC (0001) substrate contains a higher density of defects than that on the on-axis substrate (Fig. 1), both interfaces are found to have a similar density of trapped negative charge.

The SIMS depth profiles shown in Fig. 5, however, reveal that oxygen, hydrogen and carbon atoms are incorporated into the AlN and at the interface during growth. The drift of such impurity ions under the applied electric fields and at the low temperatures used here is not expected, but their presence at the interface can alter the nature of the local chemical bonds which can be at the origin of the interface traps[9]. However, more studies are currently underway to further clarify their role in determining the electrical characteristics of the interface.

IV. Summary

Metal/AlN/n–type 6H–SiC (0001) (MIS) heterostructures have been prepared by epitaxially growing wurtzite AlN layers on both vicinal and on-axis 6H–SiC (0001) substrates using GSMBE. The C-V characteristics obtained for these MIS heterostructures depend strongly on temperature in the range from 200 to 573 K, and exhibit hysteresis effects consistent with the presence of slow interface traps. The amount of hysteresis increases with decreasing temperature as a consequence of the shift of the Fermi level closer to the semiconductor conduction band, causing the emission rate to be less dependent on temperature. Despite the higher density of defects at the interface formed on the vicinal 6H–SiC (0001) substrate, both the interfaces on the vicinal and on-axis substrates are found to have a similar density of trapped negative charge of 3×10^{11} cm^{-2} at 300 K, which decreases with increasing temperature. These results indicate that the interface is of a high quality suitable for device application.

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V. Development of a System for Integrated Surface Cleaning and Oxide Formation on 6H-SiC

A. Introduction

The development of high-temperature, -power and -frequency devices based on SiC requires a more complete understanding of the oxide formation and interface characteristics. To have SiC device technology introduced into the mainstream industrial community, it is necessary that current technologies can be employed to device fabrication. Thermal oxidation of p-type SiC has led to an increase in defects that have resulted in degradation of the electrical properties. An oxide-positive space charge has been estimated to be about 1.5×10^{12} cm^{-2}, and the estimation of fast interface states is of the same order [1]. It is proposed that the Al dopant on p-type SiC is more readily redistributed in SiO$_2$, while the N dopant on n-type is not. This yields significant quantities of Al in thermally grown oxides on p-type SiC that form Al$_2$O$_3$, which may increase the number of defects in the oxide and the SiO$_2$/SiC interface [2]. The resultant oxide displays an increase in space charge, a lowering of the breakdown voltage, and an increase in both fast and slow interface state densities. By using an integrated UHV system, interfaces will be prepared with lower contaminant levels while gaining a better understanding of the SiC oxide formation process. The UHV compatible surface preparation and oxide formation system will be integrated with an advanced system that includes other processing and characterization capabilities that will allow for *in vacuo* characterization of the SiO$_2$/SiC interface followed by *ex situ* electrical characterization. Recent experiments on SiC have shown that cleaning and surface preparation of SiC is more involved than for Si [3]. It is unclear at this point whether or not it is necessary to totally remove all the oxygen from the SiC surface. It is proposed that the residual oxide from most surface preparation techniques is oxygen trapped at near-surface grain boundaries [4]. A systematic approach is underway to develop a process that will yield an electrical quality oxide on SiC.

B. Experimental Approach

The integrated system will allow for most of the characterization to be accomplished without exposing samples to the ambient. Furthermore, the processes will be characterized at various stages, thus allowing for the understanding of the entire oxidation process. A typical process is given as follows: (1) surface preparation; (2) initial insulator formation; (3) CVD insulator deposition. A schematic of the process is shown in Fig. 1. At each of these stages, a wide variety of techniques are available.

An experimental matrix has been set up to provide a systematic approach to the insulator formation process. Figure 2 lists the procedures and processes that will be used to determine the SiC/SiO$_2$ interface and deposition process. The base line procedure will be a RCA clean
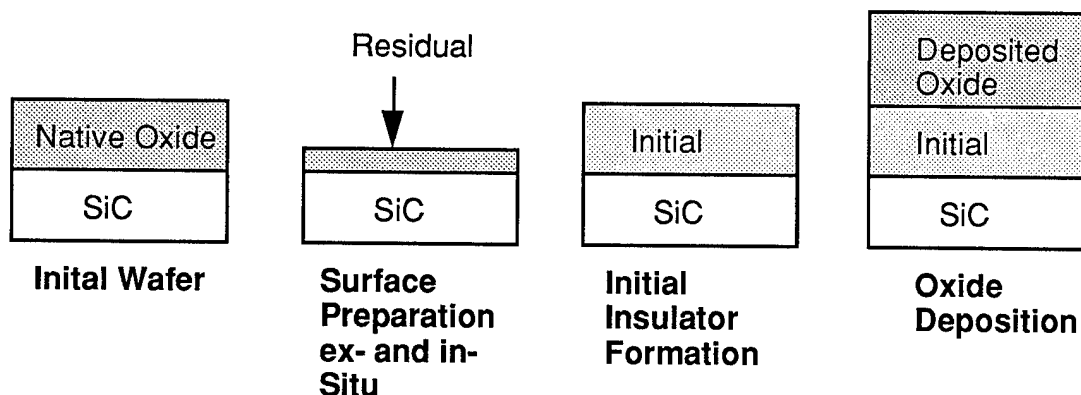
Figure 1.   Basic process for insulator formation on SiC.

ex-situ	in-situ	Initial Oxide	Insulator Deposition
RCA	None	None	Thermal CVD
RCA/HF	H-Plasma	Thermal Oxidation	Plasma CVD
RCA & pH Controlled HF	H/SiH4 Plasma	Plasma Oxidation	
RCA/HF/ UV Ozone	Excess Si/ Thermal Anneal		
RCA/Nitric	[HF Vapor]		

Figure 2.   Experimental matrix for high quality insulator formation on SiC.

followed by thermal oxide growth. The base line procedure will be compared to all other procedures. *Ex situ* surface preparation will be the first process investigated. Once the *ex situ* surface preparation technique yielding the highest quality thermal oxide has been determined, it will become the standard procedure. Using the *ex situ* preparation process previously determined as a standard process, the *in situ* surface preparation will be investigated. The *in situ* process(es) that again yield the highest quality thermal oxide will be added as a standard preparation procedure. Initial insulator formation is then investigated using the previous *ex situ* and *in situ* surface preparation techniques. Once an initial insulator formation procedure that yields a higher quality oxide is determined, it will become part of the standard preparation/growth techniques. This systematic approach will investigate the various processes and chemistries that are present in the oxidation of SiC and the SiC/SiO$_2$ interface. Surface preparation is arguably the most important step to high-quality insulator growth.

Ensuring a clean smooth surface is necessary for oxide growth. Some of the various procedures are: (1) wet chemical clean ; (2) plasma cleaning; and (3) HF vapor phase. Current cleaning techniques have been developed that will yield various levels of cleaning, specifically, most procedures cannot remove all oxygen from the SiC surface. Hydrogen plasma cleaning removes surface contaminants but leaves the residual oxide after the HF dip, see Fig. 3.
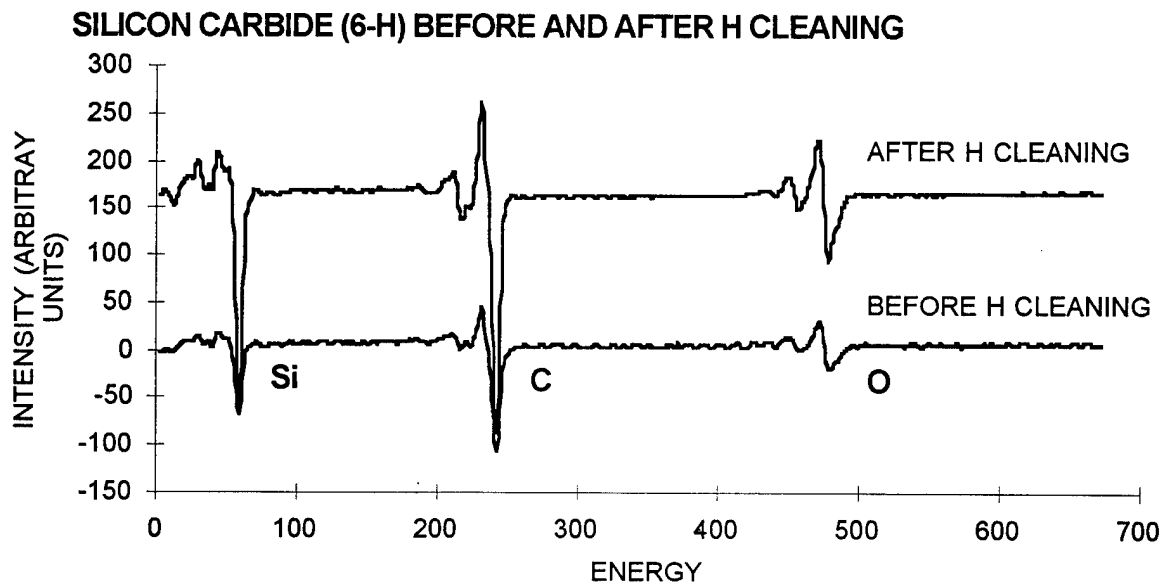
SILICON CARBIDE (6-H) BEFORE AND AFTER H CLEANING

Figure 3.   AES spectrum of 6-H SiC before and after H-plasma cleaning.

Likewise, a H/SiH$_4$ plasma has be shown to etch SiO$_2$ on Si [5] but is unable to remove the residual oxide on SiC. This is demonstrated by the Auger Spectrum in Fig. 4.
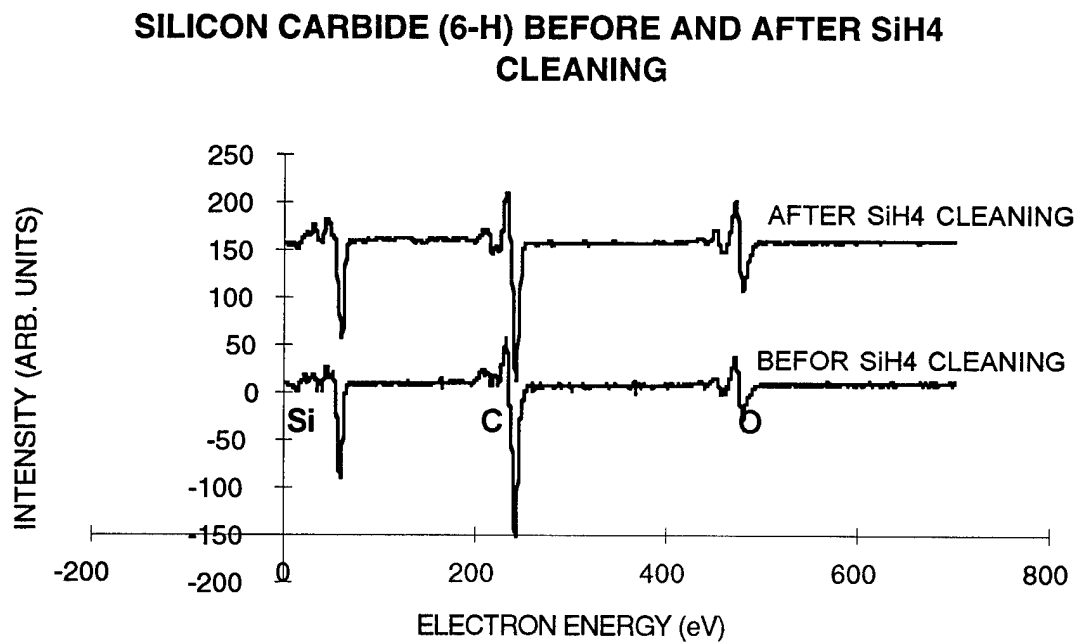
SILICON CARBIDE (6-H) BEFORE AND AFTER SiH4 CLEANING

Figure 4.   AES spectrum of 6-H SiC before and after H/SiH$_4$ plasma cleaning.

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It has not been established if this residual oxide on the SiC will result in a degradation of the electrical performance of insulators grown on it. Further investigation into the effect that the residual oxide will have on electrical characteristics is needed. As shown in previous experiments [1], it is possible to remove all the oxygen contamination within detection limits.

Insulator formation on SiC is where some of the major problems are manifested. On p-type SiC, there is considerable dopant redistribution and defect formation during the transition region between SiC/SiO_2 in thermally grown oxides. By using diverse techniques for initial insulator formation and deposited oxides, we will observe which process or combination of processes will minimize defect formation, dopant redistribution, and maximize the electrical properties on the initial oxide formation. Some of the procedures are: (1) UV ozone; (2) nitric bath; and (3) plasma enhanced CVD (PECVD). Chemical vapor deposition insulator formation is the final step in the oxide formation process. Here, oxide is deposited on the initial oxide to the desired thickness. This process is proposed to limit redistribution of dopants on p-type SiC. Deposited oxides do not have as desirable dielectric constants and can have considerable interface densities. By growing an initial oxidation layer, it is intended that the interface densities will be minimized, and traps will be reduced. Then by depositing an oxide on the deposited layer, it is aimed that there will be little dopant redistribution and a reduction of bulk charge and traps. Electrical characteristics will be determined. C-V and I-V measurements will be made to determine defects, such as trapped charge and interface charge. A primary goal of these experiments is to greatly increase the electrical characteristics of MOS structures in SiC. Ideally, we would be able to get the electrical characteristics close to those of Si, namely: a breakdown voltage of $\sim 1 \times 10^7$ V/cm, trap densities $\sim 10^{11} \text{-} 10^{10}$ cm^{-2} and interface state densities of $\sim 10^{10}$ cm^{-2}.

Currently, the oxide deposition process is characterized for the system. Oxide deposition is one of the primary focuses of the insulator formation process. The deposited oxide qualities must be maximized before any results for SiC are obtained. Via preliminary data, the deposition rate is linear with time and linear with temperature. Further investigation into other parameters, such as temperature and gas mixtures is needed to determine the best quality of deposited oxides. Preliminary electrical testing of the deposited oxides is under way. Four types of films are investigated: thermal CVD with oxygen and nitrous oxide, and PECVD with oxygen and nitrous oxide. Current oxide deposition and testing is done for Si(111) so that it maybe compared to known data. By giving a basis in silicon technology, it is thought that the transition to silicon carbide will be made more readily.

C. Results

Currently, oxide growth is being characterized and optimized. Growth rates for thermal CVD of approximately 10 Å per minute and for PECVD of 50 Å per minute are observed.

These rates are within the current parameters for gate oxide growth. The ratio of film roughness to film thickness decreases with time of growth. For thin films (<50 Å) the mean percent roughness to thickness is around 20 percent, while for thicker films (>150 Å) the mean percent roughness to thickness is around 10 percent. This is a promising result that the film uniformity may be good. Electrical testing is still needed to determine the quality of these oxides.

D. Conclusions

Current cleaning and surface preparation techniques for silicon may be inadequate in their current form for SiC. There is a residual oxide that remains after the currently accepted cleaning techniques which may or may not affect the electrical characteristics of deposited oxides. The integrated UHV system will be able to explore processes that have previously been unobtainable. The uniqueness of the surface preparation integrated with the growth and characterization system allows for capabilities that have not been previously used in the characterization and growth of oxides on SiC. Once the oxide deposition technique is well defined, focus will change to the initial oxidation procedure. The electrical characteristics will guide the selection of the optimal process and the surface diagnostics should allow a scientific understanding of the process.

E. Future Research Plans and Goals

Future goals include establishing a quality deposited oxide with good electrical characteristics equivalent to the accepted characteristics of deposited oxides. Once the procedure for oxide growth is well defined, it will enable considerable focus on the examination of the oxide layers for use as gate insulators in field effect devices. These procedures for oxide deposition on silicon will be adapted to silicon carbide. Once the deposition of oxide on silicon carbide is well known, the interface and initial oxide formation process will be examined.

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VI. Inversion Layer Mobility in SiC MOSFETs

Lateral MOSFETs have been reported by several groups on 6H-SiC [1,2] (the highest reported inversion layer mobility in the literature on fabricated MOSFETs on 6H-SiC is 72 cm^2/Vs[1]). However, lateral MOSFETs on 4H-SiC have not been reported to date. In this paper, we report the successful fabrication of lateral N-channel MOSFETs on 4H-SiC for the first time with gate-controlled output characteristics observed upto 100°C. Furthermore, we report the highest measured electron inversion layer mobilities on lateral 6H-SiC MOSFETs.

In this work, we used commercially available Al-doped P-type homo-epitaxial layers (N_A=1×10^{16} cm^{-3}) on P-type SiC substrates. The MOSFETs were fabricated using a non-selfaligned process with the drain-source nitrogen N$^+$ implants performed first and the degenerately phosphorus-doped polysilicon gate aligned to it. A 9000A thick low temperature deposited oxide (LTO) was used as the gate dielectric. The deposition temperature was 410°C and the flow-rates were 150sccm of O$_2$ and 75sccm of LTO-410 (disilane) at a chamber pressure of 750 milliTorr. The LTO was then subjected to a wet oxidation cycle at 1100°C for 400 minutes followed by an *in situ* argon anneal and re-oxidation step defined in Ref. 2. Ti/Al contacts were provided to the gate, source and drain. A large area backside Al ohmic contact was also provided. The structure of the fabricated MOSFET is shown in Fig. 1.

C-V measurements on nearby capacitors confirmed the gate dielectric thickness at 9000A and exhibited flatband voltage shifts corresponding to an effective oxide charge density of around 5×10^{11}cm^{-2}. It was calculated that this charge would reduce the threshold voltage from 25V (for a charge-free insulator) to 0V which is in agreement with measured threshold voltages of the MOSFETs. I-V measurements were performed on the MOSFETs using a Keithley Model 251 system at temperatures of 25°C, 50°C, 75°C, and 100°C. The output characteristics at 100°C of 6H-SiC and 4H-SiC lateral MOSFETs (W/L=170mm/40.5mm) are shown in Figs. 2 and 3. The threshold voltages of the MOSFETs was calculated as the intercept made to the gate-bias axis by the tangent drawn at the point of inflection of the transfer characteristics (I_{DS} vs V_{GS}). The transfer characteristics at 100°C for the FETs characterized in Figs. 2 and 3 are shown in Fig. 4. At 25°C, the threshold voltage of the MOSFETs was around 0-2V and the measured electron inversion layer mobility from the MOSFET on-resistance was 160±13 cm^2/Vs for 4H-SiC and 110±5 cm^2/Vs for 6H-SiC. The electron inversion layer mobility extracted from the MOSFET trans-conductance was 160±17 cm^2/Vs for 4H-SiC and 110±11 cm^2/Vs for 6H-SiC. The higher inversion layer mobility in 4H-SiC can be expected since the bulk mobility of electrons in the 0001 plane is greater for 4H-SiC by a factor of about 2 over 6H-SiC. The electric field dependence of the mobility was measured (Fig. 5) and the drop-off in mobility in the measured field range was only 10-15% which is less than that observed previously [1]. The electron inversion layer mobility was found to increase with temperature (Fig. 6) indicating that coulombic scattering or possibly trap-assisted transport was

the dominant factor in the mobility. The increase in the mobility with temperature was much less than has been reported previously [3].

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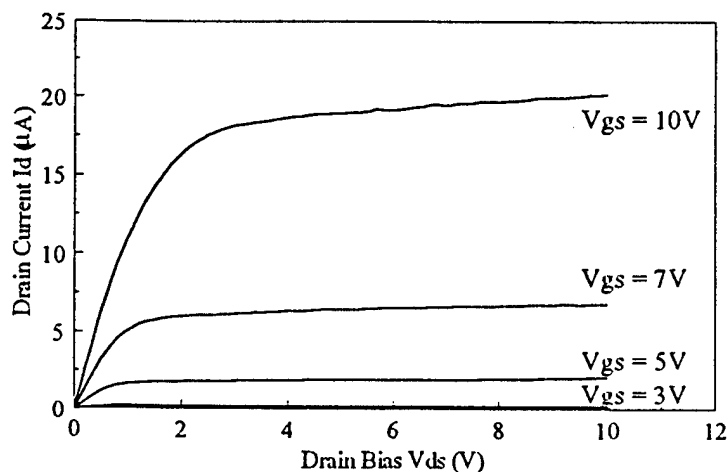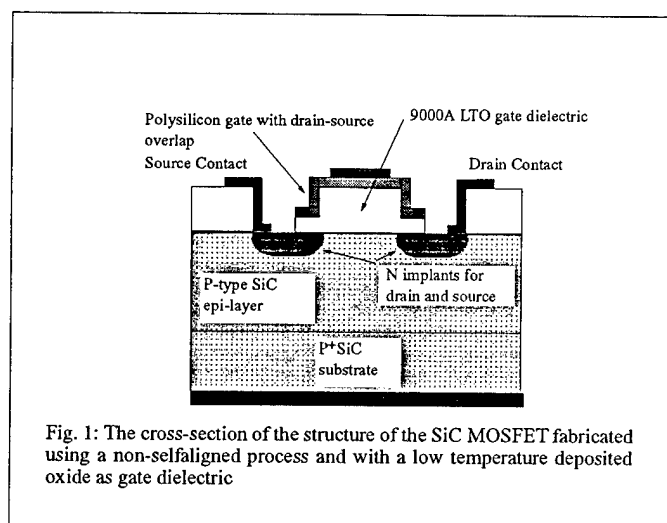3. T. Ouisse, *Proc. of ICSCRM'95*, pp. 781, 1995.

Fig. 1: The cross-section of the structure of the SiC MOSFET fabricated using a non-selfaligned process and with a low temperature deposited oxide as gate dielectric

Fig. 2: The output characteristics of a 6H-SiC lateral MOSFET (W/L = 170μm/40.5μm) at 100C fabricated using deposited oxide as the gate dielectric.

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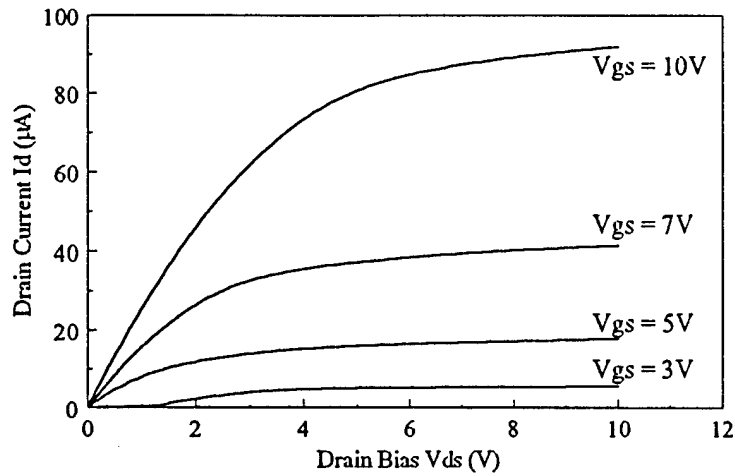
Fig. 3: The output characteristics of a 4H-SiC lateral MOSFET (W/L = 170μm/40.5μm) at 100C fabricated using deposited oxide as the gate dielectric.
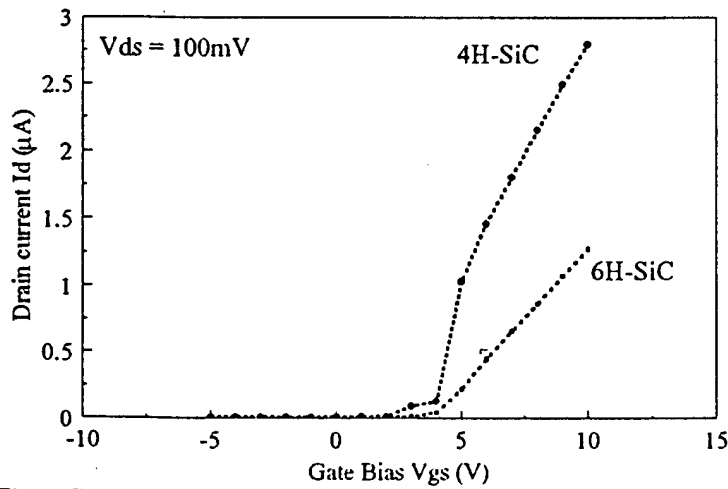
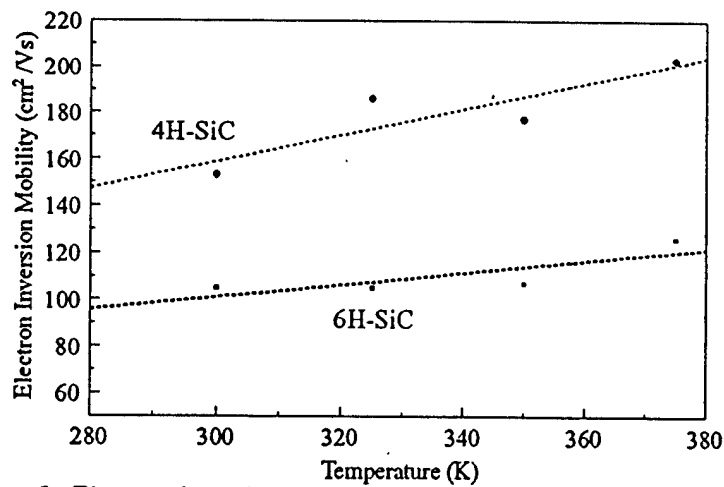Fig. 4: Transfer characteristics for SiC MOSFETs on 6H- and 4H-SiC at a drain bias of 100mV at 100C.

Fig. 5: Electron inversion layer mobilities extracted from lateral MOSFETs on 4H- and 6H-SiC as a function of temperature. The mobilities were observed to increase slightly with temperature.
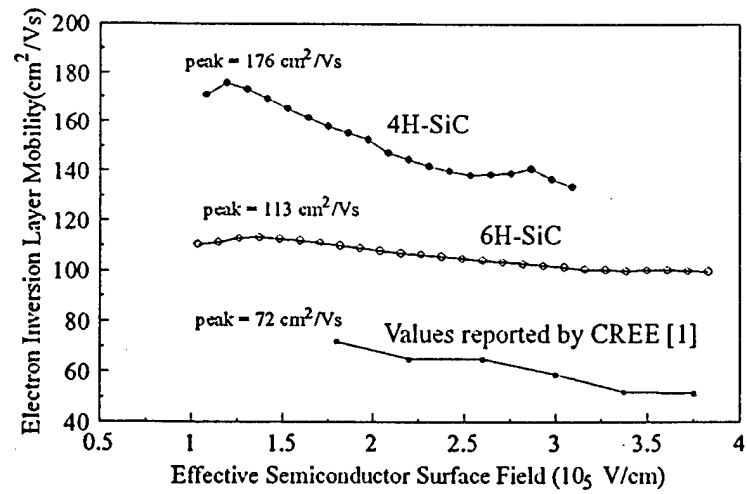
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Fig 6: The measured electron inversion layer mobilities on 4H- and
6H-SiC plotted as a function of the effective semiconductor surface
field. The best data in the literature (CREE's) is given for comparison.

VII. Measurement of Electron and Hole Impact Ionization Coefficients for SiC

Introduction

Silicon carbide has received increasing attention for power switching, microwave and high temperature applications due to its high breakdown electric field, thermal conductivity and electron saturation drift velocity. One of the most important parameters of a SiC power device is its breakdown voltage. In order to obtain a clear understanding of its breakdown characteristics, it is important to have an exact knowledge of the impact ionization coefficients for SiC. However, there is very little information available in literature for 6H-SiC (1-3) and none for 4H-SiC. In this work, measured impact ionization coefficient data for 4H and 6H-SiC are provided as a function of temperature. It is demonstrated that that the data obtained from these measurements allows a more accurate simulation of reverse breakdown voltage characteristics than that obtained using previously published data. These results have widespread utility for SiC device analysis and design.

I. Measurement Methodology

The method used in this work for measurement of impact ionization coefficients (α) is based upon the multiplication of carriers generated by a pulsed electron beam in the depletion region of a reverse biased diode. There are many important issues that need to be considered to obtain accurate measurement of α:

(1) There is electric field crowding at the edges of diodes which leads to enhanced multiplication of the carriers in this region. Since the magnitude of the electric field at the edge is not known, any carrier generation near the edges leads to errors in measurements. This problem was solved during our measurements by localizing the carrier excitation away from the diode edges using an electron beam with spot size of less than 20 μm in diameter in the center of the diode. In spite of this, any electric field crowding at the diode edges is still a major problem because this results in reducing the breakdown voltage to below the parallel plane case. This can severely limit the maximum electric field at the measurement site and reduce the range of the fields over which α can be measured. Hence, it is crucial to create a good edge termination in the diodes. In our work, a Schottky diode structure with argon ion implant edge termination (4) was used to obtain nearly ideal breakdown voltage.

(2) Defects are known to severely affect the breakdown characteristics of devices. Therefore, it is important that the measurement be made in a defect free location. In our measurements, the Electron Beam Induced Current (EBIC) technique was used to identify the location of electrically active defects. Thus, it was possible to choose a defect free region for the α measurements. Further, since the defect density of commercially available SiC wafers is known to be in the order of 10^4 cm^{-2}(5), devices were fabricated with area of less than 5 x 10^{-5} cm^2 so that at least half of the diodes were free of dislocations and micropipes.

It is necessary to extract the α from the measured multiplication rates. To achieve this, a thin drift region with a low doping density is required to obtain a nearly constant electric field profile with depth. Equations were therefore derived for the extraction of the impact ionization coefficients from the multiplication data assuming a constant electric field profile in the drift region (for a P-type Schottky diode):

$$1 - \frac{1}{M_p} = (\frac{\alpha_p}{\alpha_n - \alpha_p})[\exp(\alpha_n - \alpha_p)W - 1] \qquad (1)$$

where M_p is the multiplication due to holes and α_p and α_n are impact ionization coefficients due to electron and holes, respectively and W is the thickness of the epilayer. In a P-type Schottky diode, where ionization due to holes is dominant, it can be shown that

$$\alpha_p = \frac{\ln(M_p)}{W} \qquad (2)$$

Thus, α_p can be calculated from the measured multiplication factor M. Similar expressions were developed for electron impact ionization using N-type Schottky diode structures. In order to verify the methodology for extracting α, simulations were performed using MEDICI with and without including the impact models using the actual doping profile measured on the fabricated devices. The resulting reverse I-V characteristics and the corresponding electric field profile obtained from simulations are shown in Fig. 1 and Fig. 2, respectively.
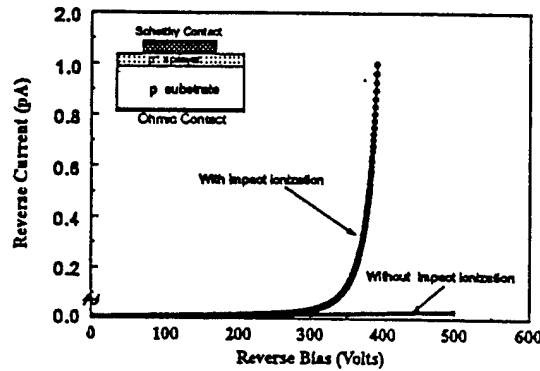
Fig. 1 Reverse IV for a 6H-SiC SBD obtained from simulations with and without impact ionization to determine multiplication rate from which α is extracted.
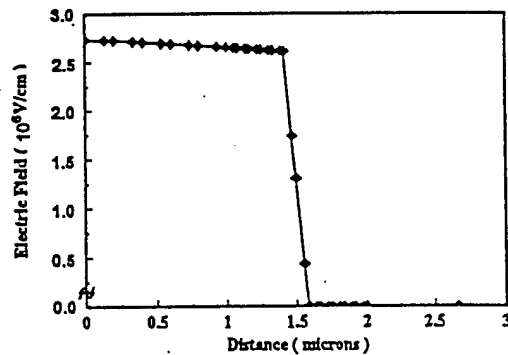

Fig. 2 The electric field profile obtained for a structure simulated is Fig. 1 showing that constant field profile is a reasonable assumption.

The multiplication factor M was then calculated by taking the ratio of the reverse current at each reverse bias value. The corresponding electric field was calculated using E = V/W. For an epitaxial layer doping of 5×10^{15} cm^{-3}, the constant electric field profile approximation was found to be a reasonable assumption as demonstrated in Fig. 3 which compares the α values extracted using this procedure with the values input into

the simulator. It can be seen that the extraction procedure works well over wide electric field range for P-type SiC due to high impact ionization rates for holes in SiC.
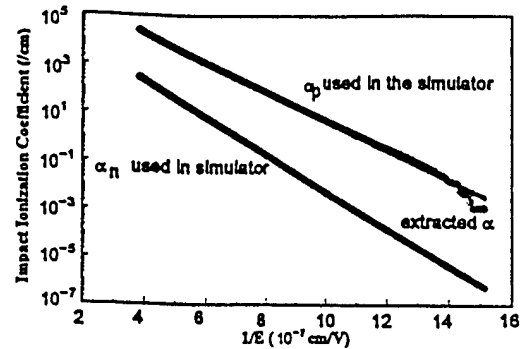

Fig. 3 α extracted for holes using analytical solution developed for a P-type SBD fits well with the values input into the simulator

However, for N-type SiC, it was found that α_n can only be extracted at smaller electric fields as shown in Fig. 4 before the onset of a strong contribution from the generated holes. For this reason, only data on α_p is reported in this paper.
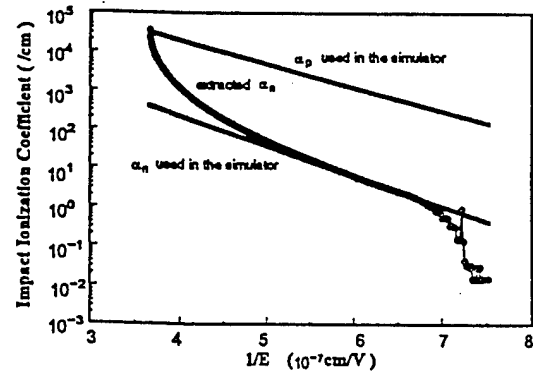

Fig. 4 α extracted for electrons using the analytical solution for a N-type SBD fits well with the value input into the simulator for low field values. However, at high fields there is onset of large contribution from holes.

II. Measurement Setup

A schematic of the impact ionization measurement setup is shown in Fig. 5. A scanning electron microscope (Hitachi S-2700) was used for the generation of carriers using the electron beam. The electron beam was pulsed using a beam blanking setup in conjunction with the scanning electron microscope. The beam blanking device essentially consists of two electrodes, placed in

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the electron gun region, which are used to deflect the beam with an externally applied bias. The external bias is a pulse produced by a pulse generator which is also input into the lock-in- amplifier as a reference. The photocurrent generated by the pulsed electron beam excitation of the reverse biased Schottky diode is tracked using the lock-in-amplifier. This current is then ploted as a function of the applied reverse bias voltage measured using a digital multimeter across the Schottky diode.
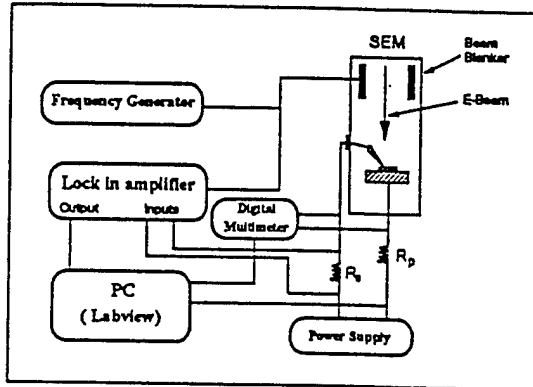

Fig. 5 Schematic of the experimental setup

A curve of the multiplication versus electric field is then obtained from this data, from which impact ionization coefficients are extracted using equation (2). The setup was interfaced with a personal computer and controlled using LABVIEW, a graphical programming tool, to allow extensive and accurate data acquisition. A heated sample stage was used to obtain α data as a function of temperature.

III. Device Fabrication and Characterization

Schottky barrier diodes were fabricated on P-type 6H and 4H-SiC (5 x 10^{15} cm^{-3}, 2 μm thick) homoepitaxial layers grown on off-axis SiC substrates (3 x10^{18} cm^{-3}). Prior to metal deposition, the SiC wafer was given a Huang clean. Schottky diodes (60-100 μm diameter) were fabricated using a shadow mask with sequential evaporation of Ti (2000 A) and Al (2000 A) layers. Blanket evaporation of a Ti/Al layer was also done on the heavily doped substrate to form a large area backside contact. An argon implant was performed around the edges to obtain nearly ideal breakdown (4). The exact doping concentration and thickness of the epitaxial layers was obtained using the C-V measurement. The forward and reverse characteristics of the diode was studied using I-V measurement. The P-type 6H and 4H-SiC were found to exhibit breakdown voltages of 530 V and 570 V, respectively.

IV. Impact Ionization Data

Typical plots of multiplication factor M at room temperature vs. bias obtained from measurements on 6H and 4H-SiC are shown in Fig. 6.
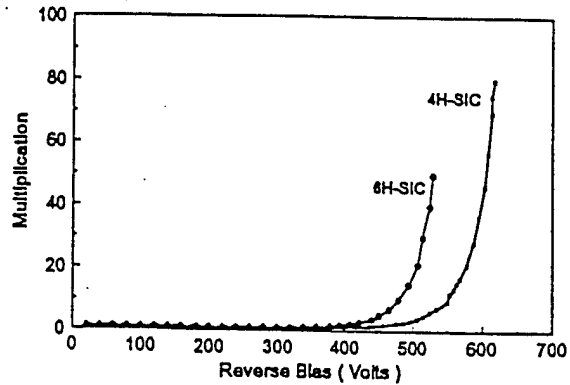

Fig. 6 Multiplication with increasing reverse bias in 4H- and 6H-SiC SBD structure

Using this data, the impact ionization coefficients for holes in 4H and 6H-SiC were obtained as a function of the electric field E as shown in Fig. 7 and Fig. 8, respectively.
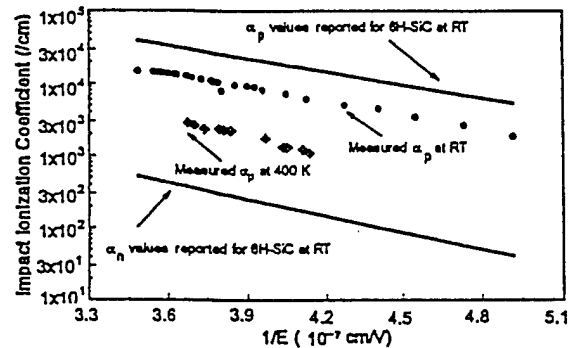

Fig. 7 Measured impact ionization coefficients for holes in 6H-SiC SBD at RT and at 400K compared to data available in literature.
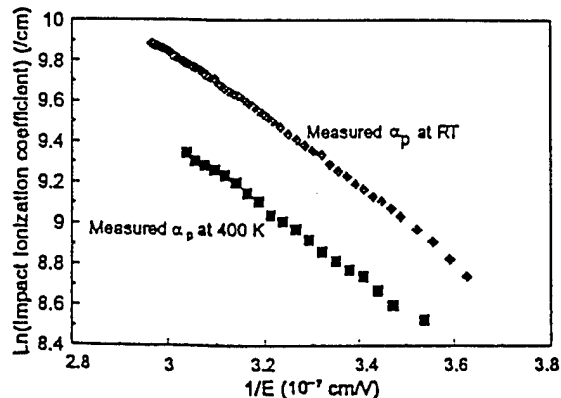

Fig. 8 Measured impact ionization coefficients for holes in 4H-SiC SBD at RT.

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Using the Van Overstraeten equation:

$$\alpha = a\, e^{-b/E} \qquad (3)$$

our measurements gave an a_p value of $(2.5 \pm 0.1) \times 10^6$ /cm and a b_p value of $(1.48 \pm 0.1) \times 10^7$ V/cm for 6H-SiC at room temperature. Values of a_p and b_p for 4H-SiC were found to be $(3.5 \pm 0.5) \times 10^6$ /cm and $(1.7 \pm 0.4) \times 10^7$ V/cm, respectively. Using the heating stage inside the SEM, impact ionization coefficient measurements were also performed at 400 K for both 4H and 6H-SiC. These measurements gave an a_p value of 1.68×10^6 /cm and a b_p value of 1.47×10^7 V/cm in 6H-SiC and an a_p value of 1.8×10^6 /cm and a b_p value of 1.65×10^7 V/cm in 4H-SiC. The α_p was found to decrease with increasing temperature (as has been observed in silicon). This indicates that the breakdown voltage of the 4H and 6H-SiC devices should increase with temperature, which is an important desirable characteristic for power devices. We therefore conclude that the previously reported (6) reduction in breakdown voltage with temperature is due to the presence of defects or edge effects. As a final corroboration of our extracted α values with the measured reverse breakdown voltages on our diodes, simulations were performed using the measured α coefficients (a and b). This gave a breakdown voltage of 520 V in 6H-SiC as shown in Fig. 9 which is the same as the experimentally observed data for 6H-SiC. In comparison, the breakdown voltage obtained using data available in literature was only 450 V.
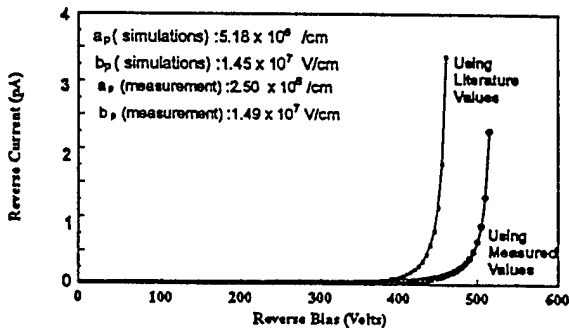
Fig. 9 Comparison of simulated reverse IV for a 6H-SBD using hole ionization coefficients available in literature and using new measured data

The critical electric field calculated from simulations using the extracted α_p parameters was found to be 3.2×10^6 V/cm as shown by the electric field profile near breakdown in Fig. 10. Simulations using the data available in literature gave lower values of 2.8×10^6 V/cm. This implies a 15% increase in the breakdown field strength (E_c) for 6H-SiC and a 20% increase in E_c for 4H-SiC. Using this data, it is shown in Table 1 that Baligas Figure of Merit (BFOM)

increases by about 1.5 x 6H-SiC and by about 1.8 x in 4H-SiC indicating even superior specific on resistance for SiC FETs than projected earlier (7).
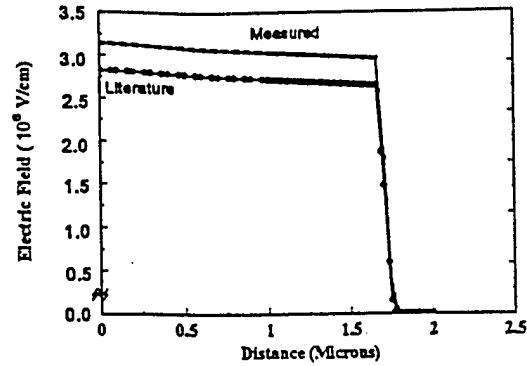
Fig. 10 Comparison of simulated electric field for a 6H-SBD using hole ionization coefficients available in literature and using new measured data

Parameters	6H-SIC	4H-SIC
Previous Ec Values	2.8×10^6 V/cm	2.8×10^6 V/cm
Previous BFOM	25	309
New Ec Values	3.2×10^6 V/cm	3.4×10^6 V/cm
New BFOM	37	553

Table. 1 Comparison of critical electric field (E_c) and Baliga's Figure of Merit (BFOM) values obtained for N-type SiC using the data available in literature and using new measured data

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